REMARKS

The Applicants have carefully considered this Application in connection with the Examiner's Action, and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-43 in the Application. In response to a restriction requirement, the Applicants previously elected Claims 1-10 and withdrew Claims 11-43 from consideration pending the filing of a Divisional Application. The Applicants subsequently canceled Claims 1-10, without prejudice or disclaimer, and added new Claims 44-53. The Applicants presently amend Claim 44 and add new Claim 54 without adding new claimed subject matter. More specifically, Claim 44 has been amended solely to comply with 35 U.S.C. §112 and to incorporate the subject matter previously recited in Claim 48. Similarly, new Claim 54 merely reflects previous Claim 44 as amended to comply with 35 U.S.C. §112 and incorporating the subject matter recited in currently pending Claim 52. The Applicants also presently cancel Claims 11-43 and 48 without prejudice or disclaimer. Accordingly, Claims 44-47 and 49-54 are currently pending in the Application.

I. Objection to Claims 44-53

The Examiner has objected to Claims 44-53 because "[o]ne can understand that the MOSFET includes a conductive substrate and a material different from the SiC tub." While the Applicants do not agree, Claim 44 has been amended solely to expedite prosecution. Consequently, the Applicants request the Examiner withdraw the objection to Claims 44-53.

II. Rejection of Claim 48 under 35 U.S.C. §112

The Examiner has rejected Claim 48 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors had possession of the claimed invention at the time the application was filed. Specifically, the Examiner asserts that there is no support for a SiC tub located within a trench, as previously recited in Claim 48, since the embodiment of FIGURE 3 does not disclose forming a trench. However, the embodiment of FIGURE 2F illustrates a trench 209 in which a SiC tub 210 is formed. Accordingly, FIGURE 2F taken together with the remainder of the present application reasonably conveys to one skilled in the art that a silicon carbide tub may be located within a trench formed in a conductive substrate, as previously recited in Claim 48 and now incorporated in independent Clam 44. Therefore, the Applicants respectfully traverse the Examiner's rejection of the subject matter of previous Claim 48 under 35 U.S.C. §112, first paragraph.

III. Rejection of Claims 44-53 under 35 U.S.C. §103

The Examiner has rejected Claims 44-53 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,896,194 to Suzuki in view of U.S. Patent No. 5,672,889 to Brown. However, the combination of Suzuki and Brown fails to support a *prima facie* case of obviousness of Claim 44 and its dependent claims because the combination fails to teach or suggest each and every element recited in Claim 44.

More specifically, the combination fails to teach a silicon carbide tub located within a trench formed in a conductive substrate, as recited in Claim 44, and as conceded by the Examiner.

(Examiner's Action, page 5). However, the Examiner asserts that it would have been obvious to a person of ordinary skill in the art to form the GaAs layer 31 in the Si substrate 32 rather than on the substrate 32, as disclosed in Suzuki. The Applicants respectfully disagree. The GaAs layer 31 cannot practically be formed in a trench in the substrate 32 because a substantial portion of the substrate 32 underlying the GaAs layer 31 is removed to form a hole 33 after the GaAs layer 31 is deposited on the substrate 32. (Column 3, lines 48-68). Forming the GaAs layer 31 in a trench in the substrate 32 and subsequently removing most of the portion of the substrate 32 under the trench would result in a device that was mechanically unsound and excessively susceptible to failure due to the lack of support of the GaAs layer 31 within the substrate 32. Thus, it is not obvious to a person of ordinary skill in the art to form the GaAs layer 31 in a trench in the substrate 32.

Brown also fails to suggest forming a silicon carbide tub within a trench formed in a conductive substrate, as recited in Claim 44 of the present application. In contrast, Brown merely teaches forming grooves 16 through at least two of three SiC layers 10, 12, 14. (Column 5, lines 9-15). Moreover, because Brown is directed toward vertical transistors instead of horizontal transistors, one skilled in the art would find no suggestion, motivation or even mere mention of forming the SiC channel layer 12 in a trench in a substrate because a channel layer formed in a trench would cover or otherwise restrict access to the underlying source or drain and render the transistor inoperable.

Accordingly, the combination of Suzuki and Brown fails to teach or suggest each and every element of Claim 44 of the present application. In view of the foregoing remarks, the combination of Suzuki and Brown fails to support a *prima face* case of obviousness of Claims 44-53 under 35

U.S.C. §103(a). Consequently, the Applicants request the Examiner withdraw the §103 rejection of Claims 44-53.

Moreover, the combination of Suzuki and Brown fails to support a *prima facie* case of obviousness of new Claim 54 and its dependent claims because the combination fails to teach or suggest each and every element recited therein. More specifically, the combination fails to teach a conductive substrate that includes a buried oxide layer formed therein, as recited in Claim 54, and as conceded by the Examiner. (Examiner's Action, page 5). However, the Examiner asserts that it would have been obvious to a person of ordinary skill in the art to form a combination of the Suzuki and Brown devices on an SOI substrate in order to improve the electrical isolation of the device. The Applicants respectfully disagree.

The specific combination asserted by the Examiner as being obvious to one skilled in the art is to form the MOSFET of Suzuki in a SiC material, as taught by Brown, instead of forming the MOSFET in a GaAs material. (Examiner's Action, page 4). However, one skilled in the art would not be motivated to employ an SOI substrate with the teachings of Suzuki, as asserted by the Examiner. (Examiner's Action, page 5). More specifically, after forming the GaAs layer 31 on the Si substrate 32, Suzuki teaches forming a hole 33 that terminates at the GaAs layer 31, wherein the sides of the hole 33 and the exposed, bottom surface of the GaAs layer 31 are subsequently lined with a metal layer 34 comprising a Ti/Au stack. (Column 5, lines 50-55). The metal layer 34 electrically connects the top and bottom sides of the device. One skilled in the art would not employ a SOI substrate or another substrate having a buried oxide layer therein when both sides of the substrate are electrically coupled to one another, because this would destroy the intended conductivity of the device. Thus, Suzuki fails to suggest employing a substrate having

a buried oxide layer formed therein, as recited in new Claim 54 of the present application. Accordingly, the Applicants respectfully traverse the Examiner's assertion that it would have been obvious to one skilled in the art to construct the Suzuki device on an SOI substrate.

Therefore, the combination of Suzuki and Brown fails to teach or suggest each and every element of new Claim 54 of the present application. In view of the foregoing remarks, the combination fails to support a *prima face* case of obviousness of new Claim 54 under 35 U.S.C. §103(a).

IV. Additional References Made of Record

The Applicants believe that the additional references made of record and not relied upon by the Examiner are not particularly pertinent to the claimed invention, but the Applicants retain the right to address these references in detail, if necessary, in the future.

V. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 44-53.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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ATTORNEY DOCKET NO.: LOTFI 22-2 **PATENT**

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Please amend Claim 44 as follows:

44. (Amended) A semiconductor device, comprising:

a lateral metal-oxide semiconductor field effect transistor (MOSFET), including:

a silicon carbide tub located within [or contacting] a trench formed in a conductive substrate [including a material different from the silicon carbide tub];

a gate formed on the silicon carbide tub; and

source and drain regions located in the silicon carbide tub and laterally offset from the gate; and

a complimentary metal-oxide semiconductor (CMOS) device formed on the conductive substrate, the CMOS device having a tub comprising [the] a material different from the silicon carbide tub.

(2) Please cancel Claims 11-43 and 48 without prejudice or disclaimer.

(3) Please add new Claim 54 as follows:

--54. (New) A semiconductor device, comprising:

a lateral metal-oxide semiconductor field effect transistor (MOSFET), including:

a silicon carbide tub located within or contacting a conductive substrate;

a gate formed on the silicon carbide tub; and

source and drain regions located in the silicon carbide tub and laterally offset from the gate; and

a complimentary metal-oxide semiconductor (CMOS) device formed on the conductive substrate, the CMOS device having a tub comprising a material different from the silicon carbide tub, and wherein the conductive substrate includes a buried oxide layer formed therein.--